



School of Information Technology and Electrical Engineering
The University of Queensland, Australia

Conference Program

2004 IEEE INTERNATIONAL CONFERENCE ON FIELD-PROGRAMMABLE TECHNOLOGY

December 6 – 8, 2004, Brisbane, Australia

Technical Co-sponsor
The IEEE Electron Devices Society

In cooperation with
The IEEE Queensland Section (Region 10)



9.00-9.15

Opening and welcome

N. Bergmann (The University of Queensland)
O. Diessel (The University of New South Wales)

9.15-10.00

1.0 Keynote:

Gordon Brebner, Xilinx

Programming a Hyper-Programmable Architecture for Networked Systems

E. Keller, G. Brebner
Xilinx Research Labs

10.00-10.50

1.1 Stream Processing

Chair: Neil Bergmann
The University of Queensland

Field Programmable Gate Array Implementation of a Generalized Decoder for Structured Low-Density Parity Check Codes

L. Sun, V. Bhagavatula (Carnegie Mellon University)

Partial Character Decoding for Improved Regular Expression Matching in FPGAs

P. Sutton (The University of Queensland)

10.50-11.20

Morning Tea

11.20-12.35

1.2 Programmable Architectures 1

Chair: Carl Ebeling
University of Washington

Interconnect Architectures for Modulo-Scheduled Coarse-Grained Reconfigurable Arrays

S. Wilton, N. Kafafi (University of British Columbia)
B. Mei, S. Vernalde (IMEC)

Directional and Single-Driver Wires in FPGA Interconnect

G. Lemieux, E. Lee, M. Tom, A. Yu (University of British Columbia)

A Greedy Algorithm for Tolerating Defective Crosspoints in NanoPLA Design

H. Naeimi, A. DeHon (CalTech)

12.35-2.00

Lunch

2.00-3.15

1.3 CAD: Synthesis, Place & Route

Chair: Rajat Moona
Indian Institute of Technology, Kanpur

SHAPER: Synthesis for Hybrid FPGAs containing PLAs using Reconvergence Analysis

R. Manimegalai, A. Manojkumar, V. Kamakoti
(Indian Institute of Technology, Madras)

Placement and Routing for Non-Rectangular Embedded Programmable Logic Cores in SoC Design

T. Wong, S. Wilton (University of British Columbia)

QuickRoute: A Fast Routing Algorithm for Pipelined Architectures

S. Li, C. Ebeling (University of Washington)

3.15-4.30

Afternoon Tea and Poster Session 1

4.30-5.45

1.4 Application accelerators

Chair: Tarek El-Ghazawi
George Washington University

An FPGA-based Othello Endgame Solver

C. Wong, K. Lo, P. Leong (The Chinese University of Hong Kong)

Real-time Detection of Line Segments Using The Line Hough Transform

N. Nagata, T. Maruyama (University of Tsukuba)

gNBX – Reconfigurable Hardware Acceleration of Self-Organizing Maps

C. Pohl, M. Franzmeier, M. Porrmann U. Rückert
(University of Paderborn)

6.00-7.30

Welcome Reception

Venue: Holt Room, UQ Student Union.

Sponsored by Xilinx

9.00 – 9.45

2.0 Keynote:

Adrian Stoica, NASA JPL

Self-Recovery Experiments in Extreme Environments Using a Field Programmable Transistor Array

A. Stoica, D. Keymeulen, V. Duong, R. Zebulum, M. Ferguson (Jet Propulsion Laboratory) T. Arslan (Edinburgh University), X. Guo (Chromatech)

9.45-10.35

2.1 Evolvable and Adaptive Hardware

Chair: Oliver Diessel
The University of New South Wales

Extended Genetic Algorithm for Codesign Optimization of DSP Systems in FPGAs

M. Savage, Z. Salcic, G. Coghill, G. Covic (University of Auckland)

A Gate-level Model for Morphogenetic Evolvable Hardware

J. Lee (Queensland University of Technology)

10.35-11.05

Morning Tea

11.05-12.20

2.2 Programmable Architectures 2

Chair: André DeHon
CalTech

A Novel CLB Architecture to Detect and Correct SEU in LUTs of SRAM-based FPGAs

S. E. Syam, V. Chandrasekhar, M. Sashikanth, V. Kakoti (Indian Institute of Technology, Madras)
V. Narayanan (Pennsylvania State University)

Using Multi-Bit Logic Blocks and Automated Packing to Improve Field-Programmable Gate Array Density for Implementing Datapath Circuits

A. Ye, J. Rose (University of Toronto)

Stream Applications on the Dynamically Reconfigurable Processor

M. Suzuki, Y. Hasegawa, Y. Yamada, N. Kaneko, K. Deguchi, H. Amano (Keio University, Graduate School of Science and Technology) *K. Anjo, M. Motomura, K. Wakabayashi, T. Toi, T. Awashima* (NEC)

12.20-12.30

ICFPT'05 Preview and invitation

12.30-1.45

Lunch

1.45-3.00

2.3 Mapping Techniques

Chair: Steve Wilton
University of British Columbia

Compiler Reuse Analysis for the Mapping of Data in FPGAs with RAM Blocks

N. Baradaran, J. Park, P. Diniz (University of Southern California / Information Sciences Institute)

Memory Optimisations for High-Resolution Imaging

T. Todman, W. Luk (Imperial College)

On the Placement and Granularity of FPGA Configurations

U. Malik, O. Diessel (University of New South Wales)

3.00-4.15

Afternoon Tea and Poster Session 2

4.15-5.30

2.4 Arithmetic

Chair: Thambipillai Srikanthan
NTU Singapore

Adaptive range reduction for hardware function evaluation

D. Lee, A. Altaf, O. Mencer, W. Luk (Imperial College)

A Scalable Hardware Architecture for Prime Number Validation

R. Cheung, A. Brown, W. Luk, P. Cheung (Imperial College London)

Coarsely Integrated Operand Scanning (CIOS) Architecture for High Speed Montgomery Modular Multiplication

M. McLoone, C. Mclvor, J. McCanny (Queens University Belfast)

6.00

Dinner (buses depart 6.00)

Venue: River Canteen, on the Boardwalk, Southbank Parklands

2004 IEEE International Conference on Field Programmable Technology

Wednesday December 8 2004

9.00-10.15

3.1 Reconfigurable Systems

Chair: Philip Leong
The Chinese University of Hong Kong

Programmable Parallel Coprocessor Architectures for Reconfigurable System on Chip

J. Williams, N. Bergmann (School of ITEE at The University of Queensland)

Windows CE for a Reconfigurable System-on-a-Chip Processor

M. George, W. Wong (National University of Singapore)

EXPRESS-1: A Dynamically Reconfigurable Platform using Embedded Processor FPGA

H. Shibamura, M. Fukuyama, D. Uchida, S. Ikeda, M. Kuga, T. Sueyoshi (Kumamoto University)

10.15-11.15

Morning Tea and Recent Advances Poster Session

11.15-12.30

3.2 Design Flows

Chair: Wayne Luk
Imperial College London

Migrating Software to Hardware in FPGAs

R. Moona (India Institute of Technology) *R. Klein* (Mentor Graphics)

The Quartus University Information Program : Enabling Advanced FPGA Research

S. Malhotra, T. Borer, D. Singh, S. Brown (Altera Corp.)

Maximizing System Performance: Using Reconfigurability to Monitor System Communications

L. Shannon, P. Chow (University of Toronto)

12.30-1.30

Lunch

1.30-2.45

3.3 Compilation

Chair: Weng Fai Wong
National University of Singapore

Using Function Folding to Improve Silicon Efficiency of Reconfigurable Arithmetic Arrays

M. Weinhardt, M. Vorbach, V. Baumgarte, F. May (PACT XPP Technologies AG)

Low FPGA Area Multiplier Blocks for Full Parallel FIR Filters

K. Macpherson, R. Stewart (University of Strathclyde)

Pipelining Designs with Loop-Carried Dependencies

H. Styles, D. Thomas, W. Luk (Imperial College)

2.45-3.45

Afternoon Tea and Recent Advances Poster Session

3.45-5.00

3.4 Cryptography

Chair: Peter Cheung
Imperial College London

Reconfigurable Hardware Implementation of Mesh Routing in Number Field Sieve Factorization

S. Bajracharya, D. Misra, K. Gaj (George Mason University), *T. El-Ghazawi* (George Washington University)

Fast Architectures For FPGA-Based Implementation of RSA Encryption Algorithm

O. Nibouche (University of Ulster)

Single-Chip FPGA Implementation of a Cryptographic Co-Processor

F. Crowe, A. Daly, T. Kerins, W. Marnane (University College Cork)

5.00-5.10

Closing Remarks

Reconfigurable Implementation of Bit-Parallel Multipliers over GF(2^m) for Two Classes of Finite Fields

J. Imaña (Complutense University of Madrid)

FPGA Implementation of Hierarchical Memory Architecture for Network Processors

Z. Liu, K. Zheng, B. Liu (Tsinghua University)

Evaluating software and hardware implementations of signal-processing tasks in an FPGA

P. Waldeck, N. Bergmann (University of Queensland)

A Scalable Architecture for Elliptic Curve Point Multiplication

K. Järvinen, M. Tommiska, J. Skyttä (Helsinki University of Technology, Signal Processing Laboratory)

An FPGA based Prototyping Platform for Imager On Chip Applications

C. Wells (Institute for System Level Integration), *E. Duncan* (STMicroelectronics), *D. Renshaw* (University of Edinburgh)

Compact Iterative FPGA Camellia Algorithm Implementations

D. Denning (Institute of System Level Integration), *J. Irvine* (Strathclyde University), *M. Devlin* (Nallatch Ltd)

An Adaptive Viterbi Decoder Based on FPGA Dynamic Reconfiguration Technology

M. Zhu, X. Qin, C. Du (University of Shenzhen), *Z. Wei* (Xi'an Institute of Technology and Engineering Science)

Single-bit Error Correction Implementation in CRC-16 on FPGA

S. Shukla, N. Bergmann (The University of Queensland)

Pre-Silicon Prototyping of a Unified Hardware Architecture for Cryptographic Manipulation Detection Codes

T.S. Ganesh (Iowa State University), *T.S.B. Sudarshan* (Birla Institute of Technology and Science), *N.K. Srinivasan, K. Jayapal* (Darmstadt University of Applied Sciences)

FPGA-acceleration of cone-beam reconstruction for the X-ray CT

D. Stsepankou, K. Kornmesser, J. Hesser, R. Männer (ICM University of Mannheim)

Interface Adaptor Logic – A New Model For Interfacing Peripherals In IP Based Designs

T. Lee, A. Lee, N. Bergmann (University of Queensland)

FPGA Implementation of Digital Upconversion using Distributed Arithmetic FIR Filters

T. Salim (La Trobe University)

FPGA Implementation of a Phased Array DBF using Polyphase Filters

T. Salim (La Trobe University)

FPGA Design of HECC Coprocessors

G. Elias, A. Miri, T. Yeap (University of Ottawa)

A Tsume-Shogi Processor Based on Reconfigurable Hardware

Y. Hori, K. Toda (National Institute of Advanced Industrial Science and Technology), *T. Maruyama* (University of Tsukuba)

An Approach to Realize Time-Sharing of Flip-Flops in Time-Multiplexed FPGAs

M. Khan, N. Miyamoto, T. Ohkawa, A. Jamak, S. Kita, K. Kotani, T. Ohmi (Tohoku University)

A Parameterizable HandelC Divider Generator for FPGAs with Embedded Hardware Multipliers

J. Hopf (University of South Australia)

Reconfigurable I/O Interface for Mobile Equipments

N. Aibe, M. Yasunaga (University of Tsukuba)

Domain Specific Reconfigurable Fabric Targeting Viterbi Algorithm

C. Zhan, S. Khawam, T. Arslan (University of Edinburgh)

A New Architecture of Field Programmable Analog Arrays for Reconfiguration Instantiation of Continuous-time Filters

J. Becker, Y. Manoli (IMTEK, University of Freiburg)

RTOS Acceleration on Soft-core Processors Using Instruction Set Customization

Z. Jin (Peking University), *M. Sindhvani, T. Srikanthan* (Nanyang Technological University)

A Rapid Prototyping Framework for Audio Signal Processing Algorithms

N. Voss, T. Eisenbach, B. Mertsching (University of Paderborn)

Cyclic Reconfiguration for Pipelined Applications on Coarse-Grain Reconfigurable Circuits

H. Fujisawa, M. Saito, M. Arai, T. Ozawa, H. Yoshizawa (Fujitsu Laboratories Ltd.)

Achieving Wide Frequency Range in an Analog FPGA

E. Schüler, L. Carro (Universidade Federal do Rio Grande do Sul)

3D Graphics Accelerator Platform for Mobile Devices

J. Kim, J. Oh, C. Jeong, J. Kim (Samsung Electronics)

Retiming Aware Clustering for Sequential Circuits

M. Eslami Dehkordi, S. Brown (University of Toronto)

A Scalable and Pipelined FPGA implementation of an OC192 WF Scheduler

A. Merhebi, O. Ait Mohamed (University of Concordia, ECE Dept.)

Wavelet Spectral Dimension Reduction of Hyperspectral Imagery on a Reconfigurable Computer

E. Aly, T. El-Ghazawi (The George Washington University), *J. Le Moigne* (NASA/Goddard Space Flight Center), *K. Gaj* (George Mason University)

Design of an Imaging System based on FPGA Technology and CMOS Imager

F. Berry, P. Chalimbaud (LASMEA)

Study on Column Wise Design Compaction for Reconfigurable Systems

H. Kalte, G. Lee (University of Western Australia), *M. Pörrmann, U. Rückert* (University of Paderborn)

Memory Specification for Reconfigurable Computing Synthesis Tools

J. Xue, P. Sutton (The University of Queensland)

Run-Time Mapping of Applications to a Heterogeneous Reconfigurable Tiled System on Chip Architecture

L. Smit, G. Smit, J. Hurink, H. Broersma, D. Paulusma, P. Wolkotte (University of Twente)

An FPGA Implementation of a modified version of the RED Algorithm

F. Fereydouni-Forouzandeh, O. Ait Mohamed (University of Concordia, ECE Dept.)

A New Reconfigurable Architecture with Smart Data Transfer Subsystems for the Intelligent Image Processing

H. Kadota, Y. Hori (Kyushu University), *A. Wakatani* (Konan University)

FPGA Architecture Extensions for Preemptive Multitasking and Hardware Defragmentation

D. Koch, A. Ahmadinia, C. Bobda (University of Erlangen-Nuremberg), *H. Kalte* (University of Western Australia)

Implementation of a Flexible RAKE Receiver in Heterogeneous Reconfigurable Hardware

G. Rauwerda, G. Smit (University of Twente)

An Improved Montgomery Modular Inversion Targeted for Efficient Implementation on FPGA

G. Meurice de Dormale, P. Bulens, J. Quisquater (UCL CryptoGroup)

Hardware/Software Co-simulation Environment for CSoC with Soft Processors.

R. Mateos (University of Alcalá de Henares)

FPGA Implementation of Spiking Neural Networks - an Initial Step towards Building Tangible Collaborative Autonomous Agents

S. Bellis, K. Razeeb, C. Saha, K. Delaney, C. O'Mathuna (NMRC Institute, University College Cork), *A. Pounds Cornish, G. de Souza, M. Colley, H. Hagras, G. Clarke, V. Callaghan* (University of Essex), *C. Argyropoulos, C. Karistianos, G. Nikiforidis* (University of Patras)

Effective System and Performance Benchmarking for Reconfigurable Computers

E. Chitalwala, T. El-Ghazawi, K. Gaj (George Washington University), *N. Alexandridis* (George Mason University), *D. Poznanovic* (SRC Computers Inc)

Scalable Structured Data Access by Combining Autonomous Memory Blocks

W. Melis, P. Cheung, W. Luk (Imperial College London)

An Investigation into the Design of High-Performance Shared Buffer Architectures based on FPGA Technology with Embedded Memory

S. O'Kane, S. Sezer (Queens University Belfast)

Switch-Box Design for Synthesizable Coarse-Grain Arrays for System-on-Chip Applications

S. Khawam, T. Arslan (University of Edinburgh, UK)